REMARKS

Present Status of the Application

The Office Action mailed November 18, 2002 rejected all presently-pending claims 1, 3-8, and 10-11. Specifically, claim 1is rejected under 35 U.S.C. 102(b) as being anticipated by Eitan, U.S. Patent No. 5,768,192. Claims 7-8 and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Endo, U.S. Patent No. 5,596,214. Claims 1, 3-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Komori et al., JP Pub. No. 2001-007230. Claims 1, 7 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa, U.S. Patent No. 6,335,554.

After entry of the foregoing amendments, claims 1, 3, 5-8 and 11 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The present invention provides a structure of a flash memory comprising an electron trapping layer, a gate and a source/drain region, wherein the electron trapping layer is formed by stacking in sequence a first oxide layer and a dielectric layer with a high dielectric constant (i.e. a dielectric constant higher than that of Si_3N_4/SiO_2, also known as NO). The dielectric is, for

Received from < 19496600809 > at 2/18/03 8:20:04 PM [Eastern Standard Time]

example, Al_2O_3, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, Ta_2O_5, Pr_2O_3 and TiO_2. The gate is arranged on the electron trapping layer, and the source/drain region is arranged on the substrate of the two lateral sides of the electron trapping layer. In addition, the band gap of the material used for the high dielectric constant dielectric layer determines whether or not a second oxide layer should be provided on the high dielectric constant dielectric layer. The second oxide layer is not needed if the band gap of the high dielectric constant dielectric layer is closer to or greater than that of silicon oxide. On the other hand, a second oxide layer is needed if the band gap is smaller than that of silicon oxide. The advantage of the present invention is that a high dielectric constant material is used as the main material for the dielectric layer. Thus, the amount of variation of the threshold voltage is greatly reduced, and data retention of the flash memory is enhanced.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,768,192 to Eitan

A preliminary discussion of differences between the technology and structure disclosed in Eitan and the present invention is appropriate. In this regard, there is a fundamental difference in the structure and technique. ***Eitan is directed to a structure of a flash memory with ONO***

Received from < 19496600809 > at 2/18/03 8:20:04 PM [Eastern Standard Time]

layer under the gate electrode. In contrast, the present invention forms an electron trapping layer under the gate electrode. The electron trapping layer consists of a first oxide layer, a dielectric layer and a second oxide layer, wherein the dielectric layer is selected from a group consisting of Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2 and Pr_2O_3. The advantage of the present invention is that a high dielectric constant material is used as the main material of the dielectric layer. Thus, the amount of variation of the threshold voltage is greatly reduced, and data retention of the flash memory is enhanced. Applicant respectfully asserts that claim 1 defines over Eitan because not every limitation of the claimed invention is taught or otherwise suggested in Eitan. In particular, respectfully assert that Eitan does not teach or otherwise disclose *"A structure of a flash memory consisting: ....the dielectric is selected from a group consisting of Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2 and Pr_2O_3;"* as recited in the amended claim 1.

For at least these reasons, Applicant respectfully assert that claims 1, and 3, 5-6 which utilize claim 1 as a base claim patentably define over Eitan. Reconsideration and withdrawal of this rejection are respectively requested.

Received from < 19496600809 > at 2/18/03 8:20:04 PM [Eastern Standard Time]

Claims 7-8 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Endo (U.S. Patent No. 5,596,214)

A preliminary discussion of differences between the technology and structure disclosed in Endo and the present invention is appropriate. In this regard, there is a fundamental difference in the structure and technique. Endo is directed to a flash memory with a first dielectric film, a second diclectric film and a gate electrode, wherein the second dielectric film comprises Ta_2O_5. Ta_2O_5 has a band gap about 4.4; while Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, ZrO_2, HfO_2, and Pr_2O_3 has higher band gaps and barrier height than Ta_2O_5. Therefore, if flash memory without the second oxide layer, the leakage of electron stored in Ta_2O_5 layer is larger than Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, ZrO_2, HfO_2, and Pr_2O_3.

Applicant respectfully submits that these claims define over Endo because not every limitation of the claimed invention is taught or otherwise suggested in Endo. In particular, respectfully assert that Endo does not teach or otherwise disclose ***"A structure of a flash memory consisting: .... the dielectric layer having the high dielectric constant is selected from a group consisting of Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, ZrO_2, HfO_2, and Pr_2O_3;"*** as recited in the amended claim 7.

Received from < 19496600809 > at 2/18/03 8:20:04 PM [Eastern Standard Time]

For at least these reasons, Applicant respectfully assert that claim 7, and 8, 11 which utilizes claim 7 as a base claim patentably define over Endo. Reconsideration and withdrawal of this rejection are respectively requested.

Claims 1, 3-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Komori et al. (JP Pub. No. 2001-007230)

A preliminary discussion of differences between the technology and structure disclosed in Komori and the present invention is appropriate. In this regard, there is a fundamental difference in the structure and technique. ***Komori is directed to a conventional nonvolatile memory such as EEPROM with a tunneling oxide layer, a floating gate, a control gate, and an ONON stacked layer between the control gate and the floating gate. During the operation, electrons are injected into/ejected from the floating gate with a voltage applied to the control gate and the source/drain region. In contrast, the present invention consists of an electron trapping layer and a gate electrode on the electron trapping layer.*** The electron trapping layer consists of a first oxide layer, a dielectric layer and a second oxide layer, wherein the dielectric layer is selected from a group consisting of Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2 and Pr_2O_3. ***During the operation, electrons are injected into/ejected from the electron trapping***

Received from < 19496600809 > at 2/18/03 8:20:04 PM [Eastern Standard Time]

layer with a voltage applied to the gate electrode and the source/drain region. Applicant respectfully assert that claim 7 define over Komori because not every limitation of the claimed invention is taught or otherwise suggested in Komori. In particular, respectfully assert that Komori does not teach or otherwise disclose ***"A structure of a flash memory consisting: ....the dielectric is selected from a group consisting of Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2 and Pr_2O_3;"*** as recited in the amended claim 1.

For at least these reasons, Applicant respectfully assert that claims 1, and 3, 5-6 which utilize claim 1 as a base claim patentably define over Komori. Reconsideration and withdrawal of this rejection are respectively requested.

Claims 1, 7 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa (U.S. Patent No. 6,335,554)

With regard to claim 1, Applicant respectfully submit that this claim define over Yoshikawa since not every limitation of the claimed invention is taught or otherwise suggested in Yoshikawa. ***Yoshikawa is directed to a flash memory with two charge trapping layer formed on both side of the gate electrode where they are perfectly electrically separated from each other through the second gate insulation film,*** as indicated in FIG 4. ***During the operation, electrons are injected into/ejected from the trapping layer with a voltage applied to the control***

Received from < 19496600809 > at 2/18/03 8:20:04 PM [Eastern Standard Time]

gate and the source/drain region. In contrast, *the present invention forms a uniform electron trapping layer entirely over the surface of semiconductor. The electron trapping layer consists of a stacked layer of a first oxide layer, a dielectric layer, and an additional second oxide layer. During the operation, electrons are injected into/ejected from the dielectric layer with a voltage applied to the control gate and the source/drain region.* There is a fundamental difference in the structure and in the electron properties. It is clear that Yoshikawa does not anticipate the present invention because Yoshikawa teaches to have the charge trapping growing on both ends of the gate instead of uniformly underneath the gate as taught in the present. Applicant respectfully assert that Yoshikawa does not teach or otherwise disclose *"A structure of a flash memory consisting: a first oxide layer ...; a dielectric layer ...; a second oxide layer ..., wherein the dielectric is selected from a group consisting of Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2 and Pr_2O_3; a gate ...; and a source/drain region ....."* as recited in the amended claim 1. Also, Yoshikawa does not teach or otherwise disclose *"A structure of a flash memory consisting: a first oxide layer ...; a dielectric layer ..., wherein the dielectric is selected from a group consisting of Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, ZrO_2, HfO_2 and Pr_2O_3; a gate ...; and a source/drain region ....."* as recited in the amended claim 7.

Received from < 19496600809 > at 2/18/03 8:20:04 PM [Eastern Standard Time]

For at least these reasons, Applicant respectfully assert that claims 1 and 3, 5-6 which utilize claim 1 as a base claim, claim 7 and 11 which utilizes claim 7 as a base claim patentably define over Yoshikawa. Reconsideration and withdrawal of this rejection are respectively requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1, 3, 5-8, and 11 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 2/18/2003

Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809

Received from < 19496600809 > at 2/18/03 8:20:04 PM [Eastern Standard Time]

Atty Docket No.: JCLA7288 Serial No.: 09/990,862

VERSION SHOWING MARKED CHANGES

In the Specifications:

Claims 4 and 10 have been canceled without prejudice or disclaimer.

Claims 1, 5-7 and 11 have been amended as follows:

1. (Twice Amended) A structure of a flash memory comprising:

a first oxide layer positioned on a substrate;

a dielectric layer having a high dielectric constant positioned on the first oxide layer;

a second oxide layer positioned on the dielectric layer having the high dielectric constant, wherein the first oxide layer, the dielectric layer having the high dielectric constant and the second oxide layer together form a charge trapping layer, wherein [a band gap of the dielectric layer having the high dielectric constant is smaller than that of silicon oxide (SiO_2)] the dielectric is selected from a group consisting of Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2 and Pr_2O_3; and

a gate located on the second oxide layer of the charge trapping layer; and

a source/drain region located at two lateral sides of the substrate.

5. (Once Amended) The structure of claim 1, the dielectric layer having the high dielectric constant is a mixture of materials selected from [a] the group consisting of [Al_2O_3,] Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, [Ta_2O_5,] and Pr_2O_3 [and TiO_2.]

Received from < 19496600809 > at 2/18/03 8:20:04 PM [Eastern Standard Time]

6. (Once Amended) The structure of claim 1, the dielectric layer having the high dielectric constant is a stacked layer having layers made of materials selected from [a] the group consisting of [Al_2O_3,] Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, [Ta_2O_5,] and Pr_2O_3 [and TiO_2].

7. (Once Amended) A structure of a flash memory comprising:

a first oxide layer positioned on a substrate;

a dielectric layer having a high dielectric constant positioned on the first oxide layer, wherein the dielectric layer and the first oxide layer together form a charge trapping layer and the dielectric layer having the high dielectric constant is [a mixture of materials] selected from a group consisting of [Al_2O_3,]Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, [La_2O_3,] ZrO_2, HfO_2, [Ta_2O_5,] and Pr_2O_3 [and TiO_2];

a gate positioned on the dielectric layer having the high dielectric constant; and

a source/drain region positioned at two lateral sides of the substrate.

11. (Once Amended) The structure of claim 7, the dielectric layer having the high dielectric constant is a mixture of materials selected from [a] the group consisting of [Al_2O_3,] Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, [Ta_2O_5,] and Pr_2O_3 [and TiO_2.]

Received from < 19496600809 > at 2/18/03 8:20:04 PM [Eastern Standard Time]